5. The application has been amended as follows:

IN THE CLAIMS:

The claims 10 and 30, have been amended as follows:

Claim 10, line 5, after "phase/frequency error estimate," -- and a second block decoder which receives the phase/frequency estimate as an input, -- has been inserted.

Claim 10, lines 10, and 11 after "excess processing power" -- based on a likelihood of phase estimation failure based on the output of the second block decoder of each of said plurality of phase locked loops, -- has been inserted. SVP 9.20.06

Claim 30, line 3, after "a unique combination of" -- initial -- has been inserted and the second "initial" has been deleted.

The claim 33 has been cancelled without prejudice.

Reasons for Allowance

6. Applicant's amendment/remarks filed April 20, 2006 (see pages 10-13) with respect to the rejection of claims 10-17, 28, 29, and the newly added claims 30-32, have been fully considered. The rejection of claims 10-17, 28, 29 and 30-32 has been withdrawn.

7. Claims 1-32 allowed.

8. The following is an examiner's statement of reasons for allowance:

The prior art of reference in combination with other claim limitations neither teaches nor renders obvious a decision directed phase locked loop circuit comprising: